# Exhibit F

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MICRON TECHNOLOGY, INC.

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

MLC INTELLECTUAL PROPERTY, LLC,

Plaintiff,

v.

MICRON TECHNOLOGY, INC.,

Defendant.

Case No. 3:14-cv-03657-SI

**DECLARATION OF JOSEPH MCALEXANDER IN SUPPORT OF MICRON'S RENEWED MOTION FOR SUMMARY JUDGMENT FOR DOUBLE PATENTING**

Date: January 25th, 2017

Time: 10:00 a.m.

Ctrm: 1, 17th Floor

Judge: Honorable Susan Illston

I, Joseph McAlexander, declare as follows:

1. I submit this Declaration in support of Micron Technology, Inc.'s Renewed Motion for Summary Judgment of Invalidity of U.S. Patent No. 5,764,571. The facts stated herein are true and of my own personal knowledge or investigation and as an expert in this field. If called to testify, I could and would testify to these facts and opinions.

**Qualifications**

2. My background and experience is summarized in my curriculum vitae, a true and correct copy of which is submitted as Exhibit 1.

3. I am the President of McAlexander Sound, Inc. I have focused my expertise to support clients in product, process, and operations analysis and investigation.

4. I hold a Bachelor's degree in Electrical Engineering from North Carolina State University in Raleigh, North Carolina.

5. I have over 43 years of experience in microcircuit and semiconductor technologies.

6. I am the named inventor on 31 issued U.S. patents and a number of foreign patents many of which are directly related to memory design and architecture.

7. I have extensive background in the field of memory devices, and I am familiar with the knowledge and capabilities of a person of ordinary skill in the art in the design of memory devices circa 1991 - 2011. Specifically, my experience in the industry during this time, and with engineers practicing in the industry during this time, informs my opinion as to the level of skill of individuals and the general state of the art.

8. I have been retained by Fish & Richardson, P.C. on behalf of Micron to provide technical analysis for this case. I am being compensated an hourly rate for my work. I will be compensated at that hourly rate for any deposition I give in this

case or if I appear as a witness during a hearing in this case. My compensation is in no way conditioned on the outcome of this action.

**Summary of Opinions**

9. I have been asked to provide an opinion as to whether the asserted claims in this case—claims 1, 9, 12, 30, 42, and 45 of U.S. Patent No. 5,764,571 (the "Asserted Claims")—are recited by, or otherwise not patentably distinct from, the claims of U.S. Patent Nos. 7,911,851 and 8,570,814.

10. As detailed below, it is my opinion that the Asserted Claims are not patentably distinct from the claims of the '851 and '814 patents.

11. At a minimum, dependent claim 7 of the '851 patent, which incorporates the limitations of claims 1, 2, and 6 of the '851 patent, claims an apparatus that recites the purported invention of each of claims 1, 9, 12, 30, 42, and 45 of the '571 patent. Additionally, at a minimum, dependent claim 3 of the '851 patent, which incorporates the limitations of claims 1 and 2 of the '851 patent, recites the purported invention of claim 1 of the '571 patent.

12. At a minimum, dependent claim 7 of the '814 patent, which incorporates the limitations of claims 1, 2, and 6 of the '814 patent, claims an apparatus that recites the purported invention of each of claims 1, 9, 12, 30, 42, and 45 of the '571 patent. Additionally, at a minimum, dependent claim 3 of the '814 patent, which incorporates the limitations of claims 1 and 2 of the '814 patent, recites the purported invention of claim 1 of the '571 patent.

**Legal Standards**

13. Although I am not an attorney, I have a basic familiarity with certain aspects of patent law, including claim construction, anticipation, obviousness, and double patenting.

14. I am informed that the claims of a patent can be subject to being invalidated in view of the doctrine of obviousness-type double patenting where they are obvious variations of the claims or otherwise not patentably distinct from another, earlier-expiring patent having a common inventor.

15. I am informed that, in the context of obviousness-type double-patenting, claims of a later-expiring patent are obvious variations of the claims of an earlier-expiring patent where any difference between the earlier-expired claims and the later-expiring claims would have been obvious to a person of ordinary skill in the art ("POSITA").

16. I am informed that, although the doctrine of obviousness-type double patenting addresses whether the *claims* of one patent are obvious over the *claims* of another patent, it is allowable to consider the specifications and file histories of the patents to determine the scope of these claims.

17. I am informed that patent claims can be independent or dependent, and that dependent claims include all limitations of the claims from which they depend.

18. I am informed that the limitations recited in a method claim can be disclosed by, or rendered obvious in view of, an apparatus claim. *In re Lonardo*, 119 F.3d 960, 968 (Fed. Cir. 1997) ("We do not agree that there is a patentable distinction between the method of using the device and the device itself. The claimed structure of the device suggests how it is to be used and that use thus would have been obvious."); *Unova Inc. v. Hewlett-Packard*, No. CV 02-3772 ER, 2006 WL 5434550, at *1 (C.D. Cal. Feb. 27, 2006) ("A claim of a method can be an obvious variation of a claim of a device if the method claimed in the later patent is obvious in light of the teachings of the earlier patent or is suggested by the device itself").

**Materials Considered**

19. I have considered the following materials in reaching my opinions in this declaration:

20. U.S. Patent No. 5,764,571 (Ex. A);

21. Prosecution history of U.S. Patent No. 5,764,571, Dkt. No. 59-9;

22. U.S. Patent No. 7,911,851 (Ex. B);

23. Prosecution history of U.S. Patent No. 7,911,851, Dkt. No. 59-11 to 59-16;

24. U.S. Patent No. 8,570,814 (Ex. C);

25. Prosecution history of U.S. Patent No. 8,570,814 (Ex. E);

26. U.S. patents related to the '571 patent;

27. Prosecution histories for U.S. patents related to the '571 patent; and

28. The parties' Joint Claim Construction and Pre-Hearing Statement, Dkt. No. 58

29. The Court's Claim Construction Order, Dkt. No. 95

**Level of Skill in the Art**

30. I understand that the Court has adopted the Plaintiff's definition of a POSITA in the early 1990s, which is one who would have had an undergraduate degree in electrical engineering (or an equivalent subject) together with three to four years of post-graduate experience designing semiconductor devices and memory devices, or a master's degree in electrical engineering (or an equivalent subject) together with one to two years of post-graduate experience in designing semiconductor devices and memory devices, wherein this description is approximate, and a higher level of education or skill might make up for less experience, and vice-versa.

31. My opinions below explain how a POSITA, under the definition adopted by the Court, would have understood the claims, technology, and references in this matter.

**Claim 1 of the '571 Patent is an Obvious Variation of Claims 7 of the '851 and '814 Patents**

32. For ease of analysis, the charts below compare the elements of the '571 patent claims to the '851 and '814 patent claims that recite the '571 elements.

33. Dependent claim 7 of the '851 patent incorporates the elements of claims 1, 2, and 6 of the '851 patent. (Ex. B) ('851 patent) at 20:5-30.

34. Dependent claim 7 of the '814 patent incorporates the elements of claims 1, 2, and 6 of the '814 patent. (Ex. C) ('814 patent) at 20:4-31.

35. The chart below compares claim element 1A of the '571 patent to claims 1 of the '851 and '814 patents.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 1A: A multi-level memory device comprising:<br><br>an electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of $K^n$ predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$; | 1. A non-volatile memory apparatus, comprising:<br><br>an electrically-alterable non-volatile memory cell having more than two predetermined memory states; a programming signal source which applies a programming signal to said memory cell;<br><br>control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell, and said control circuitry controlling the application of said programming signal to said | 1. A non-volatile memory apparatus, comprising:<br><br>an electrically-alterable non-volatile memory cell having more than two predetermined memory states; a programming signal source which applies a programming signal to said memory cell;<br><br>control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell, and said control circuitry controlling the |

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| | memory cell based on the selected programming reference parameter; | application of said programming signal to said memory cell based on the selected programming reference parameter; |

36. To a person of ordinary skill in the art ("POSITA"), a memory device stores information in a plurality of memory cells. The amount of information that the memory device can store depends at least in part on the number of memory cells in the device, as well as the number of memory states or "levels" to which each memory cell can be programmed.

37. Claims 1 of the '851 and '814 patents recite the '571 patent claim 1's requirement of a multi-level memory device because the '851 and '814 patents claim an apparatus with a memory cell that has more than two memory states.

38. Claims 1 of the '851 and '814 patents recite a memory cell "for storing" input information because the '851 and '814 patents recite applying a programming signal to a memory cell based on a selected programming reference parameter. Indeed, the purpose of a memory cell in a memory apparatus is to store information; and that storage occurs in an alterable memory by programming.

39. Claims 1 of the '851 and '814 patents recite the '571 patent's claim to storing input information in one of $K^n$ memory states, where K is the base of a predetermined number system and n is the number of bits stored per cell, and where $K^n > 2$, because the '851 and '814 patents recite a memory cell with more than two memory states. In essence, the '571 patent claim 1 recites having $K^n$ memory states and constrains that number to be "more than two." A POSITA would understand that a memory cell with more than one memory state stores information in bits. A POSITA would further understand that the mathematical relationship

recited in the '571 patent–that the number of memory states required to represent information equals the base of a number system to the power of the number of bits per cell–is inherent to any digital memory system.

40. Thus, it is my opinion that claim element 1A is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 7 of the '851 patent, which incorporates the limitations of claims 1, 2, and 6 of the '851 patent, and claim 7 of the '814 patent, which incorporates the limitations of claims 1, 2, and 6 of the '814 patent.

41. The chart below compares claim element 1B of the '571 patent to claims 1 and 6 of the '851 and '814 patents.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 1B: memory cell programming means for programming said multi-level memory cell in accordance with said input information; | 1. . . . a programming signal source which applies a programming signal to said memory cell;<br><br>control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell ….and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter; | 1. . . . a programming signal source which applies a programming signal to said memory cell;<br><br>control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell, and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter; |

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| | 6. Non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed. | 6. A non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed. |

42. Claims 1 of the '851 and '814 patents recite the '571 patent claim 1's requirement of programming a multi-level memory cell because the '851 and '814 patents recite applying a programming signal to a memory cell. When a programming signal is applied to a memory cell, the result achieved is that the memory cell is thereafter programmed. Claims 6 of the '851 and '814 patents reflect this result, insofar as they recite that a memory cell "reaches the memory state to which [it] is to be programmed."

43. Claims 1 of the '851 and '814 patents recite the '571 patent's requirement of programming a memory cell in accordance with input information because the '851 patent claims the controlled application through "control circuitry" of programming signals based on programming reference parameters, which are in turn based on information indicating a memory state to which an electrically alterable memory cell is to be programmed. This information is necessarily "input" because the memory cells on which this information is programmed are "electrically alterable," as claims 1 of the '851 and '814 patents require. A POSITA would understand that "electrically alterable" indicates that a memory cell is capable of being programmed to different states, with different input information. *See* Ex. A ('571) patent at 2:1-13 (describing non-alterable memory cells that permanently store certain information once they are manufactured).

44. Thus, it is my opinion that claim element 1B is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 7 of the '851 patent, which incorporates the limitations of claims 1, 2, and 6 of the '851 patent, and claim 7 of the '814 patent, which incorporates the limitations of claims 1, 2, and 6 of the '814 patent.

45. The chart below compares claim element 1C of the '571 patent to claims 1 of the '851 and '814 patents.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 1C: reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states; and | 1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell . . . | 1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell |

46. Claims 1 of the '851 and '814 patents recite the '571 patent claim 1's requirement of "reference voltages . . . each of said reference voltages corresponding to a different one of said predetermined memory states"—which the Court construed as "verify reference voltage(s), each verify reference voltage corresponding to a different one of the predetermined memory states"—because the '851 and '814 patents require a programming reference parameter. The '571, '851, and '814 specifications and claims 7 of the '851 and '814 patents make plain that a verify parameter or voltage is used for programming. *See, e.g.* Ex. A ('571) at 8:26-29;

Ex. B ('851) at 10:25-28; Ex. C ('814) at 10:30-33. The '851 and '814 specifications appear to have renamed "verify reference voltage" of the '571 patent as a "programming reference voltage." *Compare* Ex. A ('571) at 8:66-9:7 *with* Ex. B ('851) at 10:67-11:8 *and* Ex. C ('814) at 11:5-13. Claims 1 of the '851 and '814 patents recite that reference "parameters" are selected, which refers to a physical, measureable property. Determining a parameter from a memory cell that corresponds to the state of that cell, and comparing that parameter to a reference parameter, was well-known before the priority date of the '571 patent. *See, e.g.*, Ex. A ('571) at 5:16-30 (discussing conventional memory devices that "compare[] the voltage at [a memory cell terminal] with a reference voltage"). A POSITA would understand that, realistically, two choices exist for such a reference parameter in memory devices, voltage or current. In my experience, voltage-based systems are far more common. Indeed, the '851 and '814 patents focus almost exclusively on "voltage-based memory systems which utilize voltage signals from the memory and reference cells," and only briefly mention the possibility of current-based memory systems. Ex. B ('851) at 19:31-37; Ex. C ('814) at 19:38-43. Thus, a POSITA would understand that, in a memory system of non-volatile, electrically alterable memory, voltage would be a natural and obvious type of physical property to use as a reference parameter.

47. Claims 1 of the '851 and '814 patents recite the '571 patent claim 1's requirement of "reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information"—which the Court construed under 35 U.S.C. § 112 ¶ 6 with "verify reference select circuit" as corresponding structure for the function of "selecting one of a plurality of reference voltages in accordance with the input information"—because the '851 and '814 patents recite control circuitry that selects a programming reference parameter indicating a

memory state to which a memory cell is to be programmed. The '851 and '814 patent specifications teach that selecting a programming reference voltage is accomplished by the same "verify reference select circuit" identified as corresponding structure for the '571 patent. *See* Ex. A ('571) at 8:66-9:3; Ex. B ('851) at 10:67-11:4; Ex. C ('814) at 11:5-9. As discussed above, "input information" corresponds to a memory state to which a memory cell is to be programmed.

48. Thus, it is my opinion that claim element 1C of the '571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 7 of the '851 patent, which incorporates the limitations of claims 1, 2, and 6 of the '851 patent, and claim 7 of the '814 patent, which incorporates the limitations of claims 1, 2, and 6 of the '814 patent.

49. The chart below compares claim element 1D of the '571 patent to claims 2 of the '851 and '814 patents.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 1D: comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage, | 2. Non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter. | 2. A non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter. |

50. Claims 2 of the '851 and '814 patents, which include all limitations of claims 1 of the '851 and '814 patents, respectively, recite the '571 patent claim 1's requirement of comparing a voltage of a multi-level memory cell with a selected reference voltage—which is a portion of a claim term the Court construed under 35 U.S.C. §

112 ¶ 6 with the "comparator" as corresponding structure for the function of "comparing a voltage of the multi-level memory cell with the selected reference voltage, and for further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to the input information"—because claims 2 of the '851 and '814 patents recite a comparator that compares a parameter of a memory cell with a selected (programming) reference parameter. A POSITA would understand that the '851 and '814 patents' disclosure of comparing a parameter corresponding to the state of a memory cell encompasses the '571 patent's disclosure of comparing the voltage of a memory cell. In addition, as explained further below, Claims 3 of the '851 and '814 patents demonstrate that it would have been obvious to use voltage as the reference parameter used.

51. Thus, it is my opinion that claim element 1D of the '571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 7 of the '851 patent, which incorporates the limitations of claims 1, 2, and 6 of the '851 patent, and claim 7 of the '814 patent, which incorporates the limitations of claims 1, 2, and 6 of the '814 patent.

52. The chart below compares claim element 1E of the '571 patent to claims 6 and 7 of the '851 patent.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 1E: said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information. | 6. Non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed.<br><br>7. Non-volatile memory apparatus according to claim 6, wherein the | 6. A non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed.<br><br>7. A non-volatile memory apparatus according to claim 6, |

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| | application of said programming signal is stopped in response to the change of state of the output of said comparator. | wherein the application of said programming signal is stopped in response to the change of state of the output of said comparator. |

53. Claims 6 and 7 of the '851 and '814 patents, which include all limitations of claims 1 and 2 of the '851 and '814 patents, respectively, recite the '571 patent claim 1's requirement of indicating whether the state of a multi-level memory cell is the state corresponding to said input information. These claims (6 and 7 of the '851 and '814 patents) recite a comparator with an output that changes state after a given memory cell reaches the memory state to which it is to be programmed. Because the programming signal is stopped in response to the change of state of the comparator, a POSITA would understand that the purpose of the comparator is to generate a control signal that "indicates" that the memory cell has reached the state to which it was to be programmed. At this point, the programming signal ceases to be applied because programming has been successfully completed, as recited by claims 7 of the '851 and '814 patents.

54. Thus, it is my opinion that claim element 1E of the '571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 7 of the '851 patent, which incorporates the limitations of claims 1, 2, and 6 of the '851 patent, and claim 7 of the '814 patent, which incorporates the limitations of claims 1, 2, and 6 of the '814 patent.

55. Thus, it is my opinion that claim 1 of the '571 patent is invalid for obviousness type double patenting in view of claim 7 of the '851 patent, which depends from claims 1, 2, and 6 of the '851 patent, and claim 7 of the '814 patent, which depends from claims 1, 2, and 6 of the '814 patent.

**Claim 1 of the '571 Patent is an Obvious Variation of Claims 3 of the '851 and '814 Patents**

56. For ease of analysis, the charts below compare the elements of the '571 patent claims to the '851 and '814 patent claims that recite the '571 elements.

57. Dependent claim 3 of the '851 patent depends from claims 1 and 2 of the '851 patent. (Ex. B) ('851 patent) at 20:5-13.

58. Dependent claim 3 of the '814 patent depends from claims 1 and 2 of the '814 patent. (Ex. C) ("814 patent) at 20:4-13.

59. Claim elements 1A and 1B of the '571 patent are recited by claims 1 and 2 of the '851 and '814 patents for the reasons provided above. Accordingly, claims 3 of the '851 and '814 patents recite claim elements 1A and 1B of the '571 patent.

60. The chart below compares claim element 1C of the '571 patent to claims 1 and 3 of the '851 and '814 patents.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 1C: reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states; and | 1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell . . .<br><br>3. Non-volatile memory apparatus according to claim 2, wherein said programming reference parameters and said | 1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell<br><br>3. A non-volatile memory apparatus according to claim 2, wherein said programming reference parameters and said parameter corresponding to the |

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| | parameter corresponding to the state of said memory cell are voltages. | state of said memory cell are voltages. |

61. Claims 1 and 3 of the '851 and '814 patents recite the '571 patent claim 1's requirement of "reference voltages . . . each of said reference voltages corresponding to a different one of said predetermined memory states"—which the Court construed as "verify reference voltage(s), each verify reference voltage corresponding to a different one of the predetermined memory states"—because the '851 and '814 patents require a programming reference parameter. The '571, '851, and '814 specifications make plain that a verify parameter or voltage refers to programming. *See, e.g.* Ex. A ('571) at 8:26-29; Ex. B ('851) at 10:25-28; Ex. C ('814) at 10:30-33. Claims 1 of the '851 and '814 patents recite that reference "parameters" are selected, which refers to a physical, measureable property. A POSITA would understand that, in a memory system of non-volatile, electrically alterable memory, voltage would be a natural type of physical property to use as a reference. Claims 3 of the '851 and '814 patents specifically recite voltage as the reference parameter used.

62. Claims 1 and 3 of the '851 and '814 patents recite the '571 patent claim 1's requirement of "reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information"—which the Court construed under 35 U.S.C. § 112 ¶ 6 with "verify reference select circuit" as corresponding structure for the function of "selecting one of a plurality of reference voltages in accordance with the input information"—because the '851 and '814 patents recite control circuitry that selects a programming reference voltage indicating a memory state to which a memory cell is to be programmed. The '851 and '814 patent specifications teach that selecting a programming reference voltage

is accomplished by the same "verify reference select circuit" identified as corresponding structure for the '571 patent. *See* Ex. A ('571) at 8:66-9:3; Ex. B ('851) at 10:67-11:4; Ex. C ('814) at 11:5-9. As discussed above, "input information" corresponds to a memory state to which a memory cell is to be programmed.

63. Thus, it is my opinion that claim element 1C of the '571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 3 of the '851 patent, which incorporates the limitations of claims 1 and 2 of the '851 patent, and claim 3 of the '814 patent, which incorporates the limitations of claims 1 and 2 of the '814 patent.

64. The chart below compares claim element 1D of the '571 patent to claims 2 and 3 of the '851 and '814 patents.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 1D: comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage, | 2. Non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter.<br><br>3. Non-volatile memory apparatus according to claim 2, wherein said programming reference parameters and said parameter corresponding to the state of said memory cell are voltages. | 2. A non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter.<br><br>3. A non-volatile memory apparatus according to claim 2, wherein said programming reference parameters and said parameter corresponding to the state of said memory cell are voltages. |

65. Claims 2 and 3 of the '851 and '814 patents, which include all limitations of claims 1 of the '851 and '814 patents, respectively, recite the '571 patent claim 1's requirement of comparing a voltage of a multi-level memory cell with a selected reference voltage—which is a portion of a claim term the Court construed under 35 U.S.C. § 112 ¶ 6 with the "comparator" as corresponding structure for the function of "comparing a voltage of the multi-level memory cell with the selected reference voltage, and for further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to the input information"—because claim 2 of the '851 and '814 patents recite a comparator that compares a parameter of a memory cell with a selected (programming) reference parameter. A POSITA would understand that the '851 and '814 patents' disclosure of comparing a parameter corresponding to the state of a memory cell encompasses the '571 patent's disclosure of comparing the voltage of a memory cell. Claims 3 of the '851 and '814 patents, which includes the limitations of claims 1 and 2 of the '851 and '814 patents, respectively, recite that these parameters are voltages.

66. Thus, it is my opinion that claim element 1D of the '571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 3 of the '851 patent, which incorporates the limitations of claims 1 and 2 of the '851 patent, and claim 3 of the '814 patent, which incorporates the limitations of claims 1 and 2 of the '814 patent.

67. The chart below compares claim element 1E of the '571 patent to claims 2 of the '851 and '814 patents.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 1E: said comparator means further generating a control signal indicating whether the state of | 2. Non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a | 2. A non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which |

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| said multi-level memory cell is the state corresponding to said input information. | comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter. | compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter. |

68. Claims 2 of the '851 and '814 patents, which include all limitations of claims 1 of the '851 and '814 patents, recite the requirement of claim element 1E of the '571 patent for generating a control signal indicating whether the state of a multi-level memory cell is the state corresponding to said input information. Claims 2 of the '851 and '814 patents recite a comparator that compares the state of the memory cell with a selected programming reference parameter. Claims 2 of the '851 and '814 patents further require that control circuitry controls the application of a programming signal to the memory cell based on that same selected programming reference parameter. A POSITA would understand that a comparator is a device that compares at least two electric or electronic parameters. A comparator outputs one signal where the first of these parameters is greater than the second parameter, and the comparator outputs a different signal where the second of these parameters is greater than the first parameter. A POSITA would further understand that, by comparing the parameter of a memory cell to a reference parameter, the comparator will effectively "indicate whether" or "verify that" a memory cell has been programmed to the state corresponding to the selected reference parameter.

69. Thus, it is my opinion that claim element 1E of the '571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 2 of the '851 patent, which incorporates the limitations of claim 1 of the '851 patent, and claim 2 of the '814 patent, which incorporates the limitations of claim 1 of the '814 patent.

70. Thus, it is my opinion that claim 1 of the '571 patent is invalid for obviousness type double patenting in view of claim 3 of the '851 patent, which depends from claims 1 and 2 of the '851 patent, and claim 3 of the '814 patent, which depends from claims 1 and 2 of the '814 patent.

**Claims 9, 12, and 30 of the '571 Patent are Each Obvious Variations of Claims 7 of '851 and '814 Patents**

71. For ease of analysis, the charts below compare the elements of the '571 patent claims to the '851 and '814 patent claims that recite the '571 elements.

72. Dependent claim 7 of the '851 patent incorporates the elements of claims 1, 2, and 6 of the '851 patent. (Ex. B) ('851 patent) at 20:5-30.

73. Dependent claim 7 of the '814 patent incorporates the elements of claims 1, 2, and 6 of the '814 patent. (Ex. C) ('814 patent) at 20:4-31.

74. The chart below compares claim elements 9A, 12A, and 30A of the '571 patent to claims 1 of the '851 and '814 patents.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 9A/12A: Multi-level memory apparatus, comprising: an electrically alterable non-volatile memory cell having more than two predetermined memory states;<br><br>30A: Apparatus for programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, comprising: | 1. A non-volatile memory apparatus, comprising: an electrically-alterable non-volatile memory cell having more than two predetermined memory states; | 1. A non-volatile memory apparatus, comprising: an electrically-alterable non-volatile memory cell having more than two predetermined memory states; |

75. Claims 1 of the '851 and '814 patents recite the '571 patent's requirement of a multi-level memory apparatus for programming a memory cell with more than two

memory states. A POSITA would understand that an apparatus comprising memory cells with multiple memory states is itself a multi-level memory apparatus, per claim elements 9A and 12A of the '571 patent. A POSITA would also understand that an apparatus containing electrically-alterable memory cells is intended for programming those memory cells, as recited in claim element 30A of the '571 patent.

76. Thus, it is my opinion that each of claim elements 9A, 12A, and 30A of the '571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 7 of the '851 patent, which incorporates the limitations of claim 1, 2, and 6 of the '851 patent, and claim 7 of the '814 patent, which incorporates the limitations of claim 1, 2, and 6 of the '814 patent.

77. The chart below compares claim elements 9B, 12B, and 30B of the '571 patent to claims 1 of the '851 and '814 patents.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 9B: a selecting device which selects one of a plurality of predetermined reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;<br><br>12B/30B: a selecting device which selects one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a | 1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell | 1. … control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding |

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|---|---|---|
| different memory state of said memory cell; | | to a different memory state of the memory cell |

78. Claims 1 of the '851 and '814 patents recite the '571 patent's requirement of "reference signals . . . each reference signal corresponding to a different memory state of said memory cell"—which the Court construed as "reference signal(s), each reference signal corresponding to a different memory state of the memory cell"—because the '851 and '814 patents require a programming reference parameter. A POSITA would understand that the "reference signals" recited in the claim elements of the '571 patent are synonymous with the "reference parameters" of the '851 and '814 patents.

79. Claims 1 of the '851 and '814 patents recite the '571 patent's requirement of "a selecting device which selects one of a plurality of [predetermined] reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed" —which the Court construed under 35 U.S.C. § 112 ¶ 6 with "verify reference select circuit, pictured as example only in Fig. 8 as item 222" as corresponding structure for the function of "selecting one of a plurality of [predetermined] reference signals that corresponds to a memory state to which the memory cell is to be programmed"—because the '851 and '814 patents recite control circuitry that selects a programming reference parameter. Because claims 1 of the '851 and '814 patents recite that reference parameters are generated before they are subsequently selected and used, the '851 and '814 patents necessarily claim that the selected reference signal is "predetermined." The '851 and '814 patent specifications teach that selecting a programming reference voltage is accomplished by the same "verify reference select circuit" identified as

corresponding structure for the '571 patent. *See* Ex. A ('571) at 8:66-9:3; Ex. B ('851) at 10:67-11:4; Ex. C ('814) at 11:5-9.

80. Thus, it is my opinion that each of claim elements 9B, 12B, and 30B of the '571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 7 of the '851 patent, which incorporates the limitations of claims 1, 2, and 6 of the '851 patent, and claim 7 of the '814 patent, which incorporates the limitations of claims 1, 2, and 6 of the '814 patent.

81. The chart below compares claim elements 9C, 12C, and 30C of the '571 patent to claims 1 of the '851 and '814 patents.

| **'571 Claim Language** | **'851 Claim Language** | **'814 Claim Language** |
|---|---|---|
| 9C/12C: a programming signal source which applies a programming signal to said memory cell; and<br><br>30C: a programming signal source to apply a programming signal to said memory cell; and | 1. . . . a programming signal source which applies a programming signal to said memory cell; | 1. . . . a programming signal source which applies a programming signal to said memory cell; |

82. Claims 1 of the '851 and '814 patents recite the same limitation described in claim elements 9C, 12C, and 30C of the '571 patent. The Court's adoption of plain and ordinary meaning as the construction of this term does not alter this fact.

83. Thus, it is my opinion that each of claim elements 9C, 12C, and 30C of the '571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 7 of the '851 patent, which incorporates the limitations of claim 1, 2, and 6 of the '851 patent, and claim 7 of the '814 patent, which incorporates the limitations of claim 1, 2, and 6 of the '814 patent.

84. The chart below compares claim element 9D of the '571 patent to claims 1, 2, 6, and 7 of the '851 and '814 patents.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 9D: a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information. | 1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell, and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter….<br><br>2. Non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter.<br><br>6. Non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed.<br><br>7. Non-volatile memory apparatus according to claim 6, wherein the application of said programming signal is stopped in response to the change of state of the output of said comparator. | 1. … control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell, and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter….<br><br>2. A non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter.<br><br>6. A non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed.<br><br>7. A non-volatile memory apparatus according to claim 6, wherein the application of said programming signal is stopped in |

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| | | response to the change of state of the output of said comparator. |

85. As explained above with respect to the discussion of claim element 1D of the '571 patent, claims 1 and 2 of the '851 and '814 patents recite the '571 patent's requirement of a comparator that compares a parameter of a memory cell with a reference parameter. As explained above with respect to claim elements 9B, 12B, and 30B, this reference parameter is the same as the "signal" or "reference signal" recited in the '571 patent.

86. Claims 1, 2, 6, and 7 of the '851 and '814 patents recite the '571 patent's requirement of using a comparator to verify whether a memory cell is programmed to a state indicated by input information. As explained above with respect to the discussion of claim elements 1D and 1E of the '571 patent, a POSITA would understand that the comparator recited in the '851 and '814 patents is designed to indicate when a memory cell has reached a desired state. Such a person would further understand that this functionality is synonymous with "verifying" whether a memory cell has reached a desired memory state.

87. The Court's construction of "a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information" as plain and ordinary meaning does not alter my conclusions regarding this claim element of the '571 patent.

88. Thus, it is my opinion that claim element 9D of the '571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 7 of the '851 patent, which incorporates the limitations of claims 1, 2, and 6 of the

'851 patent, and claim 7 of the '814 patent, which incorporates the limitations of claims 1, 2, and 6 of the '814 patent.

89. The chart below compares claim element 12D of the '571 patent to claims 1, 2, 6, and 7 of the '851 patent.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 12D: a verifying device which detects a parameter indicating the state of said memory cell and which verifies whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal. | 1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell, and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter….<br><br>2. Non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter.<br><br>6. Non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory | 1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell, and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter….<br><br>2.A non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter.<br><br>6. A non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the |

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| | state to which said memory cell is to be programmed.<br><br>7. Non-volatile memory apparatus according to claim 6, wherein the application of said programming signal is stopped in response to the change of state of the output of said comparator. | memory state to which said memory cell is to be programmed.<br><br>7. A non-volatile memory apparatus according to claim 6, wherein the application of said programming signal is stopped in response to the change of state of the output of said comparator. |

90. Claims 1, 2, 6, and 7 of the ’851 and ’814 patents recite the ’571 patent’s requirement of “a verifying device which detects a parameter indicating the state of said memory cell and which verifies whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal”—which the Court construed under 35 U.S.C. § 112 ¶ 6 with a “comparator” as corresponding structure for the function of “detecting a parameter indicating the state of said memory cell and verifying whether the memory cell is programmed to the state indicated by said input information based on the detected parameter and the selected reference signal.” As explained above, with respect to the discussion of claim elements 1D, 1E, and 9D, the ’851 and ’814 patents recite a comparator, which is used to perform verification operations on the state of a memory cell as compared to a selected programming reference parameter. The ’851 and ’814 patents further recite “detecting a parameter” of a memory cell. A POSITA would understand that comparing a parameter of a memory cell to some different parameter necessarily entails detecting that parameter of a memory cell in the first place.

91. Thus, it is my opinion that claim element 12D of the ’571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 7 of the ’851 patent, which incorporates the limitations of claims 1, 2, and 6 of the

’851 patent, and claim 7 of the ’814 patent, which incorporates the limitations of claims 1, 2, and 6 of the ’814 patent.

92. The chart below compares claim element 30D of the ’571 patent to claims 1, 2, 6, and 7 of the ’851 and ’814 patents.

| ’571 Claim Language | ’851 Claim Language | ’814 Clam Language |
|---|---|---|
| 30D: a control device to control the application of said programming signal to said memory cell based on the selected reference signal. | 1. . . . a programming signal source which applies a programming signal to said memory cell; control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell ….and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter;<br><br>2. Non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter.<br><br>6. Non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed. | 1. . . . a programming signal source which applies a programming signal to said memory cell; control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell, and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter; |

| | | |
|---|---|---|
| | 7. Non-volatile memory apparatus according to claim 6, wherein the application of said programming signal is stopped in response to the change of state of the output of said comparator. | |

93. Claims 1, 2, 6, and 7 of the ’851 and ’814 patents recite the ’571 patent’s requirement of a control device to control the application of said programming signal to said memory cell based on the selected reference signal. In particular, claims 1 of the ’851 and ’814 patents recite this limitation almost verbatim, except that they refer to the word “parameter” rather than its synonym “signal,” as explained above with respect to claim elements 9B, 12B, and 30B and they refer to the phrase “control circuitry” rather than “control device.”

94. The Court’s construction of “control device to control the application of said programming signal to said memory cell based on the selected reference signal” as plain and ordinary meaning does not alter my conclusions regarding this claim element of the '571 patent.

95. Thus, it is my opinion that claim element 30D of the ’571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claims 1, 2, 6, and 7 of the ’851 patent, and claims 1, 2, 6, and 7 of the ’814 patent.

96. Thus, it is my opinion that claims 9, 12, and 30 of the ’571 patent are each invalid for obviousness type double patenting in view of claim 7 of the ’851 patent, which depends from claims 1, 2 and 6 of the ’851 patent, and claim 7 of the ’814 patent, which depends from claims 1, 2 and 6 of the ’814 patent.

**Claims 42 and 45 of the ’571 Patent are Each Obvious Variations of Claims 7 of ’851 and ’814 Patents**

97. For ease of analysis, the charts below compare the elements of the ’571 patent claims to the ’851 and ’814 patent claims that recite the ’571 elements.

98. Dependent claim 7 of the '851 patent incorporates the elements of claims 1, 2, and 6 of the '851 patent. (Ex. B) ('851 patent) at 20:5-30.

99. Dependent claim 7 of the '814 patent incorporates the elements of claims 1, 2, and 6 of the '814 patent. (Ex. C) ('814 patent) at 20:4-31.

100. The chart below compares claim elements 42A and 45A of the '571 patent to claims 1 of the '851 and '814 patents.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 42A/45A: A method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising: | 1. A non-volatile memory apparatus, comprising: an electrically-alterable non-volatile memory cell having more than two predetermined memory states; a programming signal source which applies a programming signal to said memory cell; | 1. A non-volatile memory apparatus, comprising: an electrically-alterable non-volatile memory cell having more than two predetermined memory states; a programming signal source which applies a programming signal to said memory cell; |

101. Claims 1 of the '851 and '814 patents recite claim elements 42A and 45A of the '571 patent for the same reasons discussed above regarding claim element 1A.

102. I am informed that the limitations recited in a method claim can be disclosed by or rendered obvious in view of an apparatus claim. *In re Lonardo*, 119 F.3d 960, 968 (Fed. Cir. 1997) ("We do not agree that there is a patentable distinction between the method of using the device and the device itself. The claimed structure of the device suggests how it is to be used and that use thus would have been obvious."); *Unova Inc. v. Hewlett-Packard*, No. CV 02-3772 ER, 2006 WL 5434550, at *1 (C.D. Cal. Feb. 27, 2006) ("A claim of a method can be an obvious variation of a claim of a device if the method claimed in the later patent is obvious in light of the teachings of the earlier patent or is suggested by the device itself").

103. Thus, it is my opinion that each of claim elements 42A and 45A of the '571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 7 of the '851 patent, which incorporates the limitations of claims 1, 2 and 6 of the '851 patent, and claim 7 of the '814 patent, which incorporates the limitations of claims 1, 2 and 6 of the '814 patent.

104. The chart below compares claim elements 42B and 45B of the '571 patent to claims 1 of the '851 and '814 patents.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 42B/45B: selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell; | 1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell | 1. . . . control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell |

105. Claims 1 of the '851 and '814 patents recite claim elements 42B and 45B of the '571 patent for the same reasons discussed above regarding claim element 1C.

106. The Court's construction of "selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed" as "selecting one of a plurality of reference signals that

corresponds to a memory state to which the memory cell is to be programmed" does not alter my conclusions regarding this claim element of the '571 patent.

107. Thus, it is my opinion that each of claim element 42B and 45B of the '571 patent is recited, by or otherwise contains minor linguistic differences that are obvious in view of, claim 7 of the '851 patent, which incorporates the limitations of claims 1, 2, and 6 of the '851 patent, and claim 7 of the '814 patent, which incorporates the limitations of claims 1, 2, and 6 of the '814 patent.

108. The chart below compares claim elements 42C and 45C of the '571 patent to claims 1 of the '851 and '814 patents.

| '571 Claim Language | '851 Claim Language |
|---|---|
| 42C/45C: applying a programming signal to said memory cell; | 1. . . . a programming signal source which applies a programming signal to said memory cell; |

109. Claims 1 of the '851 and '814 patents recite claim elements 42C and 45C of the '571 patent for the same reasons discussed above regarding claim element 1B.

110. The Court's construction of "applying a programming signal to said memory cell" as plain and ordinary meaning does not alter my conclusions regarding this claim element of the '571 patent.

111. Thus, it is my opinion that each of claim element 42C and 45C of the '571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 7 of the '851 patent, which incorporates the limitations of claims 1, 2, and 6 of the '851 patent, and claim 7 of the '814 patent, which incorporates the limitations of claims 1, 2, and 6 of the '814 patent.

112. The chart below compares claim element 42D of the '571 patent to claims 1 (incorporated into dependent claim 2), 2, 6, and 7 of the '851 and '814 patents.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 42D: detecting a parameter indicating the state of said memory cell; and<br><br>verifying whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal. | 2. Non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter.<br><br>6. Non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed.<br><br>7. Non-volatile memory apparatus according to claim 6, wherein the application of said programming signal is stopped in response to the change of state of the output of said comparator. | 2. A non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter.<br><br>6. A non-volatile memory apparatus according to claim 2, wherein an output of said comparator changes state after said memory cell reaches the memory state to which said memory cell is to be programmed.<br><br>7. A non-volatile memory apparatus according to claim 6, wherein the application of said programming signal is stopped in response to the change of state of the output of said comparator. |

113. As explained above with respect to the discussion of claim elements 1D and 9D of the '571 patent, claims 1, 2, 6, and 7 of the '851 and '814 patents recite the '571 patent's requirement of verifying whether a memory cell has been programmed to a particular state based on a parameter of a memory cell and a selected reference signal.

114. As explained above with respect to the discussion of claim element 12D, claims 1, 2, 6, and 7 of the '851 and '814 patents recite "detecting a parameter" indicative of a memory cell state.

115. The Court's construction of "verifying whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal" as "verifying whether the memory cell is programmed to the memory state indicated by comparing an indicator of the memory state with the selected reference signal" does not alter my conclusions regarding this claim element of the '571 patent. In fact, this construction clarifies that the '571 "verifying" claim term involves "comparing" as explicitly recited by the '851 and '814 patents.

116. Thus, it is my opinion that claim element 42D of the '571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 7 of the '851 patent, which incorporates the limitations of claims 1, 2, and 6 of the '851 patent, and claim 7 of the '814 patent, which incorporates the limitations of claims 1, 2, and 6 of the '814 patent.

117. The chart below compares claim element 45D of the '571 patent to claims 1 and 2 of the '851 and '814 patents.

| '571 Claim Language | '851 Claim Language | '814 Claim Language |
|---|---|---|
| 45D: and controlling the application of said programming signal to said memory cell based on the selected reference signal. | 1. . . . a programming signal source which applies a programming signal to said memory cell; control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell . . . and said control circuitry controlling the application of said programming signal to said memory cell based on the selected programming reference parameter; | 1. . . . a programming signal source which applies a programming signal to said memory cell; control circuitry which generates a plurality of programming reference parameters and selects among said plurality of programming reference parameters in accordance with information indicating a memory state to which said memory cell is to be programmed, each programming reference parameter corresponding to a different memory state of the memory cell, and said control circuitry controlling the application of said |

| | | |
|---|---|---|
| | 2. Non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter. | programming signal to said memory cell based on the selected programming reference parameter;<br><br>2. A non-volatile memory apparatus according to claim 1, wherein said control circuitry includes a comparator which compares said parameter corresponding to the state of said memory cell with the selected programming reference parameter. |

118. Claims 1 and 2 of the ’851 and ’814 patents recite claim element 45D of the ’571 patent for the same reasons discussed above regarding claim elements 1D and 1E.

119. The Court’s construction of “controlling the application of said programming signal to said memory cell based on the selected reference signal” as plain and ordinary meaning does not alter my conclusions regarding this claim element of the ’571 patent.

120. Thus, it is my opinion that claim element 45D of the ’571 patent is recited by, or otherwise contains minor linguistic differences that are obvious in view of, claim 7 of the ’851 patent, which incorporates the limitations of claims 1, 2, and 6 of the ’851 patent, and claim 7 of the ’814 patent, which incorporates the limitations of claims 1, 2, and 6 of the ’814 patent.

121. Thus, it is my opinion that claims 42 and 45 of the ’571 patent are invalid for obviousness type double patenting in view of claim 7 of the ’851 patent and claim 7 of the ’814 patent.

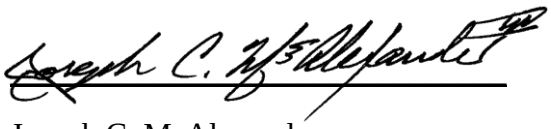
**Conclusion**

122. For the reasons given above, it is my opinion that claims 1, 9, 12, 30, 42, and 45 of the ’571 patent are each invalid for obviousness-type double patenting in view of claims 3 and 7 of the ’851 patent and claims 3 and 7 of the ’814 patent.

**Reservation of rights**

123. This declaration expresses my opinions with respect to a single issue in the case, before the deadlines for serving expert reports. I reserve the right to supplement or modify my opinions as to this issue, including if the Court modifies its constructions of the '571 claim terms, adopts new constructions, or modifies the level of ordinary skill in the art applicable to the '571 patent. I also reserve the right to provide additional opinions related to other case issues.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. Executed at Richardson, Texas, this 16th day of December 2016.



Joseph C. McAlexander